REMARKS

In the above-identified Office action, the Examiner has rejected claims 9 and 10 as failing to comply to the written description requirement. The Examiner has noted that Applicant claimed less than 500°C wherein the specification read 500°C or less. Applicant has amended the claims so they now read up to 500°C which therefore includes 500°C as required by the Examiner.

Claims 9-13 have been rejected under 35 U.S.C. 103(a) as unpatentable over Furuya et al. The Examiner has stated that Furuya et al discloses a low temperature heat treatment of 350°C-450°C and also discloses a low temperature heat treatment at 650°C-950°C, with a ramping rate of .5-2.0°C per minute. Applicant has amended claim 9 and 10 so that they now clarify the differences between the invention and the cited art of Furuya. Applicant disagrees with the Examiner's interpretation of Furuya, noting that Furuya's abstract essentially summarizes the procedure set forth in more detail in paragraphs 007-011. Further, Furuya has the purpose of controlling the DZ layer, while Applicants herein are trying to manufacture high quality silicon single crystal wafers, and do not focus on a single layer. As stated in the abstract of Furuya, the silicon wafer is first heat treated at 1150°C and then it is subject to a ramping heat treatment starting at 350°C-450°C to control the DZ layer width; this is substantially different from Applicant's claimed method in which the initial heat treatment is up to 500°C and then it is ramped to a second heat treatment of 700°C-900°C. As, specifically stated in the translated specification in paragraph 0007 "heat treatment is performed for a silicon wafer at 1150°C... then Ping heat treatment with an initiation temperature of 350°C-450°C is performed. Furthermore, heat treatment of 24 hours is performed, for example at 1000°C." Accordingly, the heat treatment of Furuya appears to be a three step process with an initial heat treatment of 1150°C. This is

substantially different from that recited in claims 9 and 10 in the first and second steps. As a result, Applicant believes claims 9 and 10 are distinguished over Furuya. With regard to claims 10 and 11, the Examiner has stated that the claims differ from the cited art only in the intended use. However, as set forth above, the prior art does not teach a first heat treatment up to 500°C with a second heat treatment of 700°C-900°C nor does it teach a first heat treatment in controlling a temperature ramping rate from the heat treatment to a higher second heat treatment in the range of 700°C-900°C. Accordingly, Furuya does not make obvious claims 10 and 11.

"Perfect Crystal" and "DZ layer" are different from each other as follows ("perfect crystal" and "DZ layer" are defined on page 23, line 17 through page 24, line 8 of the specification).

"Perfect Crystal" is a crystal free from grown-in defects. Perfect crystal is obtained by controlling the pull-up sped and/or temperature during crystal growth. In the perfect crystal, however, oxide precipitate nuclei exist. These oxide precipitate nuclei are taken into the perfect crystal during the growth. With the heat treatment of the wafer, the oxide precipitate nuclei are grown into the oxide precipitates. The oxide precipitates are used in the gettering of heavy metals.

Generally, "DZ layer" is a surface layer of the wafer in which oxide precipitates have been removed. The target to remove at the time of forming the DZ layer is oxide precipitates, not grown-in defects. The cited references also do not show the concept of removing grown-in defects.

Furuya et al. and Bischoff et al. concerns the two-stage heat treatment that is commonly employed at present in the oxide precipitate density control. In the two-stage heat treatment, oxygen in the surface layer of the wafer is diffused in the outer directions to form a DZ layer in the first-stage high-temperature heat treatment, and oxide precipitates are grown to form a oxide precipitation layer in the second-stage low-temperature heat treatment.

Neither Furuya et al. or Bischoff et a. describes or suggests the technology of the present invention in which only the second-stage heat treatment is performed independently. Further, none of them describes or suggest the technology of the present invention in which the distribution of the oxide precipitates in the oxide precipitation layer is made uniform. In other words, neither Furuya et al. nor Bischoff et al. associates the heat treatment of wafer with the distribution of the oxide precipitates.

Claims 12-13 being dependent upon claims 9 and 12 respectively, such claims are also considered allowable.

Claims 9-11 have been rejected as being unpatentable over Bischoff, et al. The Examiner has stated that Bischoff teaches heating from 450°C-800°C and then annealing at a low temperature of 400°C-500°C and heating to 750°C-1000°C. The Examiner has stated that these are overlapping ranges, and therefore, Applicant's invention would be obvious.

Applicant disagrees with the Examiner's interpretation of Bischoff, noting that Bischoff first has a high temperature cycle which is stated to be "carried out at any temperature above 1000°C", column 3 lines 7-8. As set forth in column 3, line 35, "the process proceeds to the low temperature cycle" where there is an annealment at a low temperature of 400°C-500°C and then a second high temperature of 750°C-1000°C. this is different from the subject invention as recited in claims 9-11 where there is a first heat treatment of up to 500°C and a second heat treatment of 700°C-900°C. This is substantially different from Bischoff which has a three step procedure starting off at a high temperature which Applicant does not reach in any of his heat treatment steps. As a result, Applicant believes that claims 9-11 recite over Bischoff.

Claims 9-13 have been rejected as unpatentable over Furuya or Bischoff in view of Iida, et

al or Adachi et al. As the Examiner has stated that Furuya or Bischoff discuss all of the limitations of claims 9-11 as set forth previously in the Office Action, but the Examiner states that the exception being that the wafer is single crystalline, which may be inherent, however, if not inherent, then Iida teaches a single crystal wafer with very few crystal defects. However, since Iida, Furuya and now Bischoff teach as the Examiner has stated, their combination with Iida does not provide the necessary teachings and accordingly, Applicant believes that claims 9-13 are patentable over the combination of Furuya or Bischoff and Iida or Adachi.

Applicant hereby requests reconsideration and re-examination thereof.

With the above amendments and the remarks, this application is considered ready for allowance, and Applicants earnestly solicit an early notice of same. If the Examiner believes that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned attorney at the telephone number listed below

Respectfully submitted,

WELSH & KATZ, LTD.

By
Gerald T. Shekleton
Registration No. 27,466

Dated: October 29, 2004

Welsh & Katz, Ltd.
120 South Riverside Plaza, 22nd Floor
Chicago, Illinois 60606
Telephone: 312/655-1500